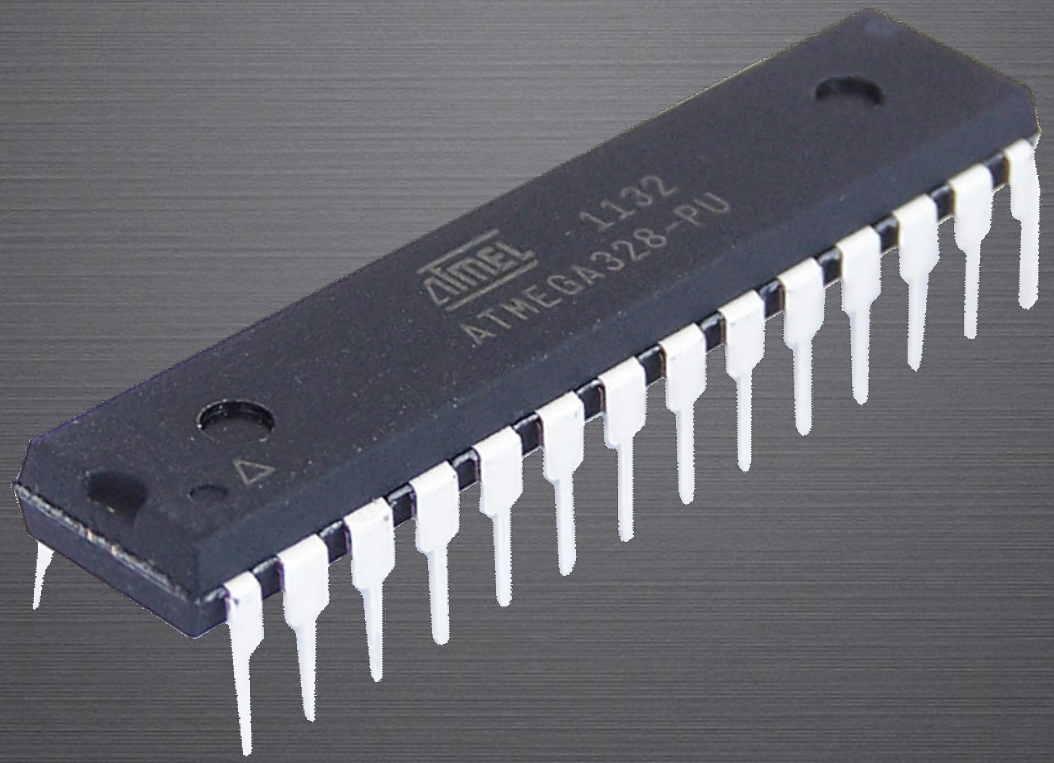
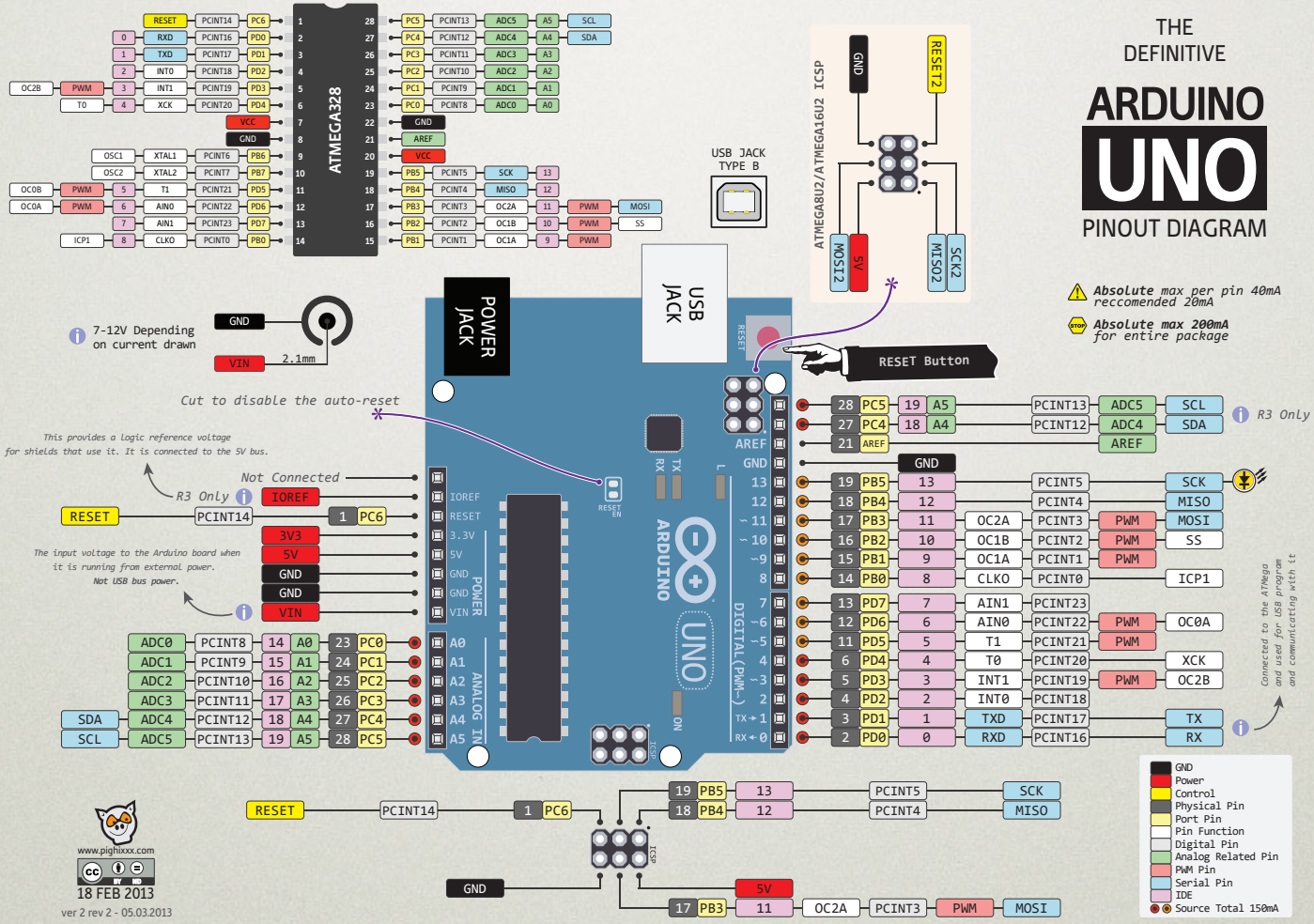
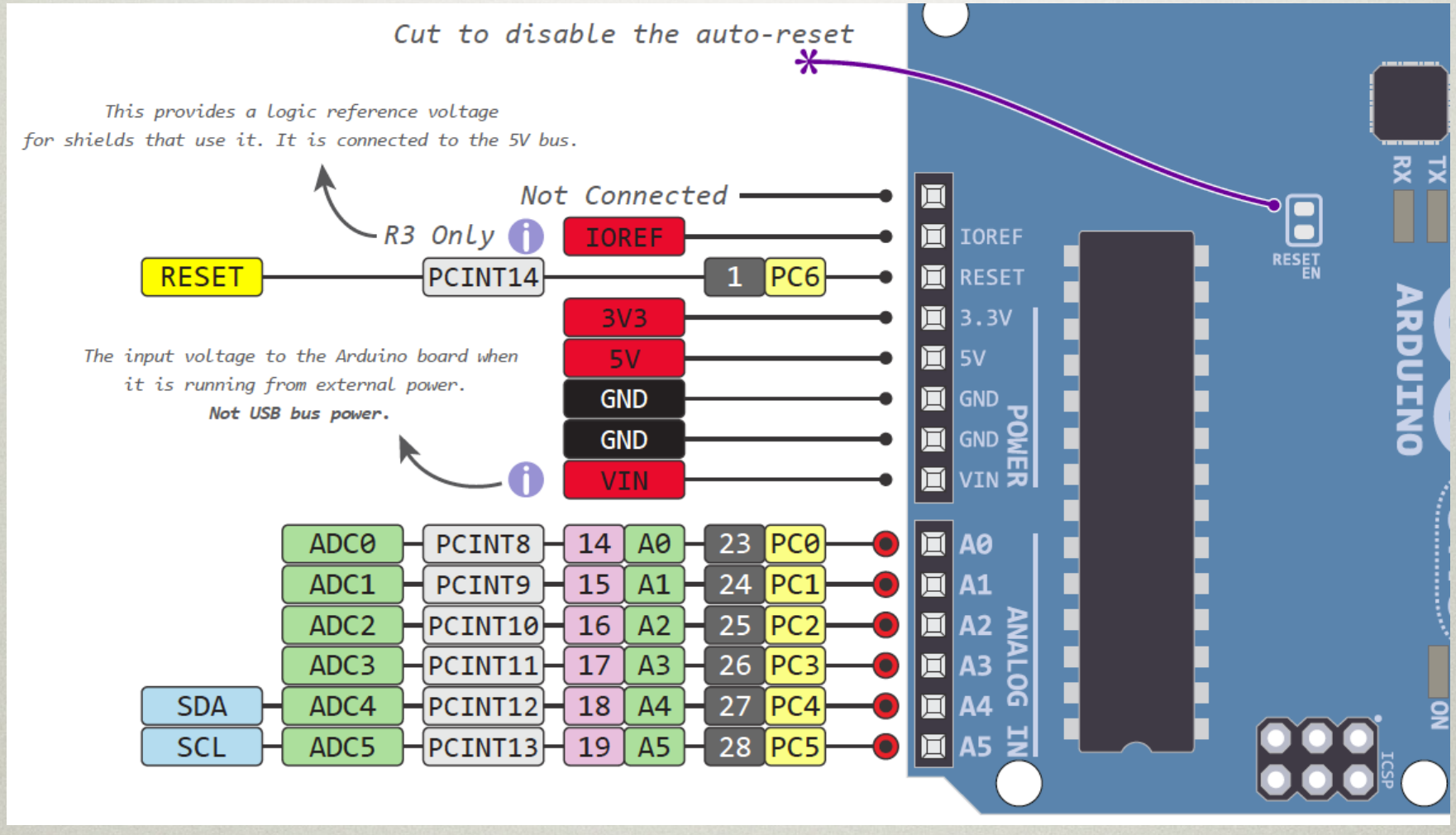


Lecture 6
Overview of the ATMega328

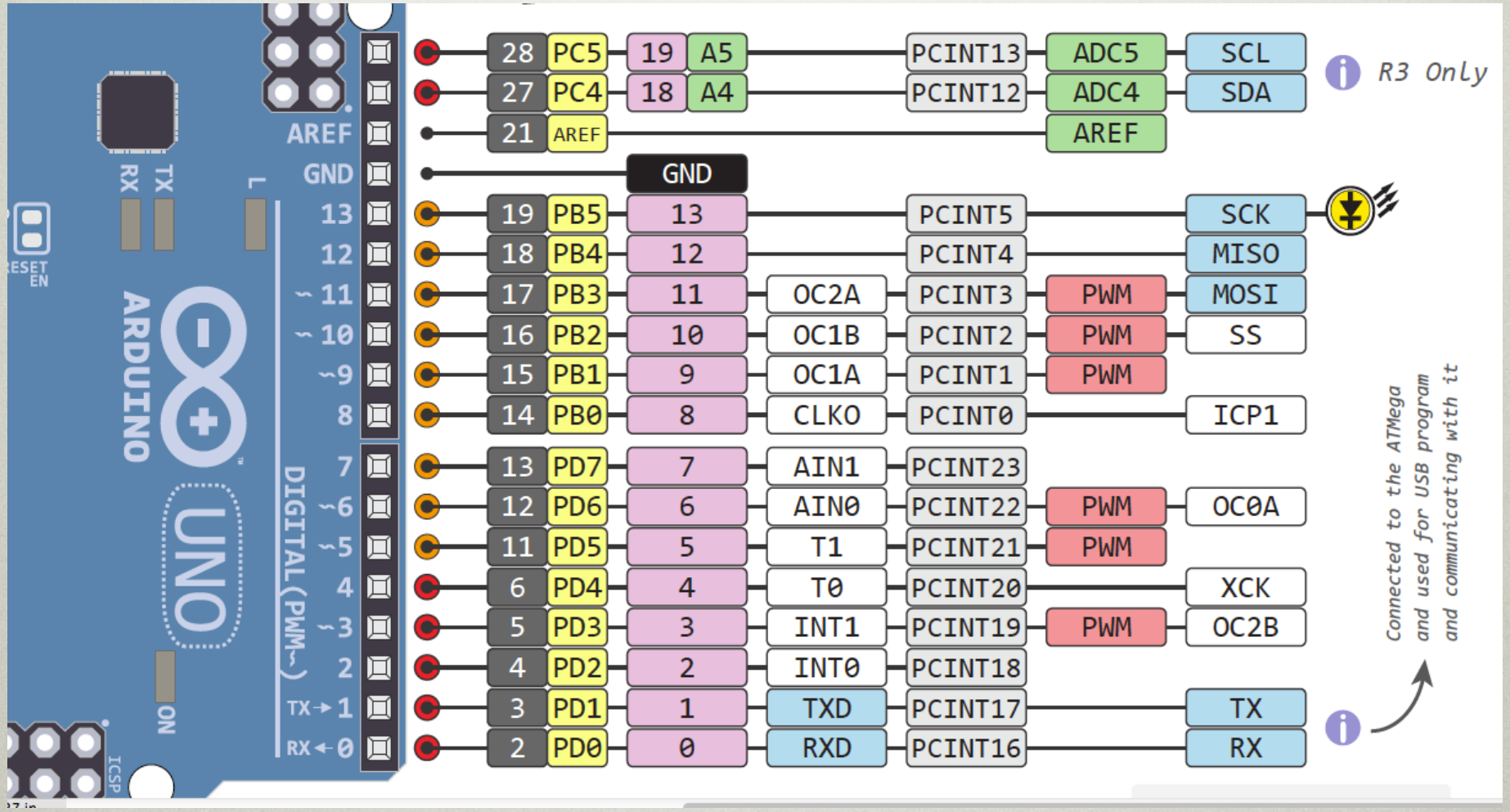
Arduino Connections



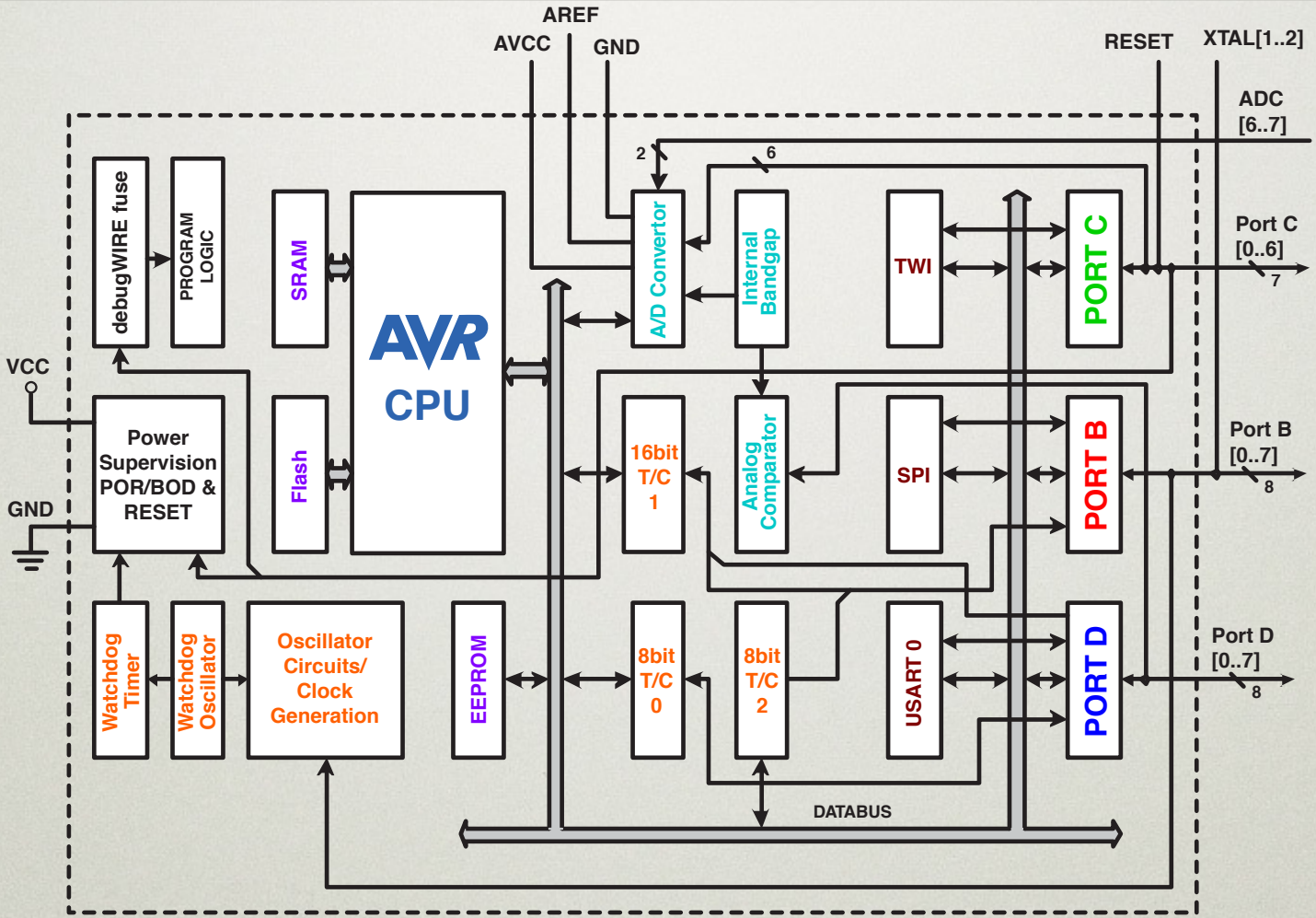
Arduino Connections



Arduino Connections



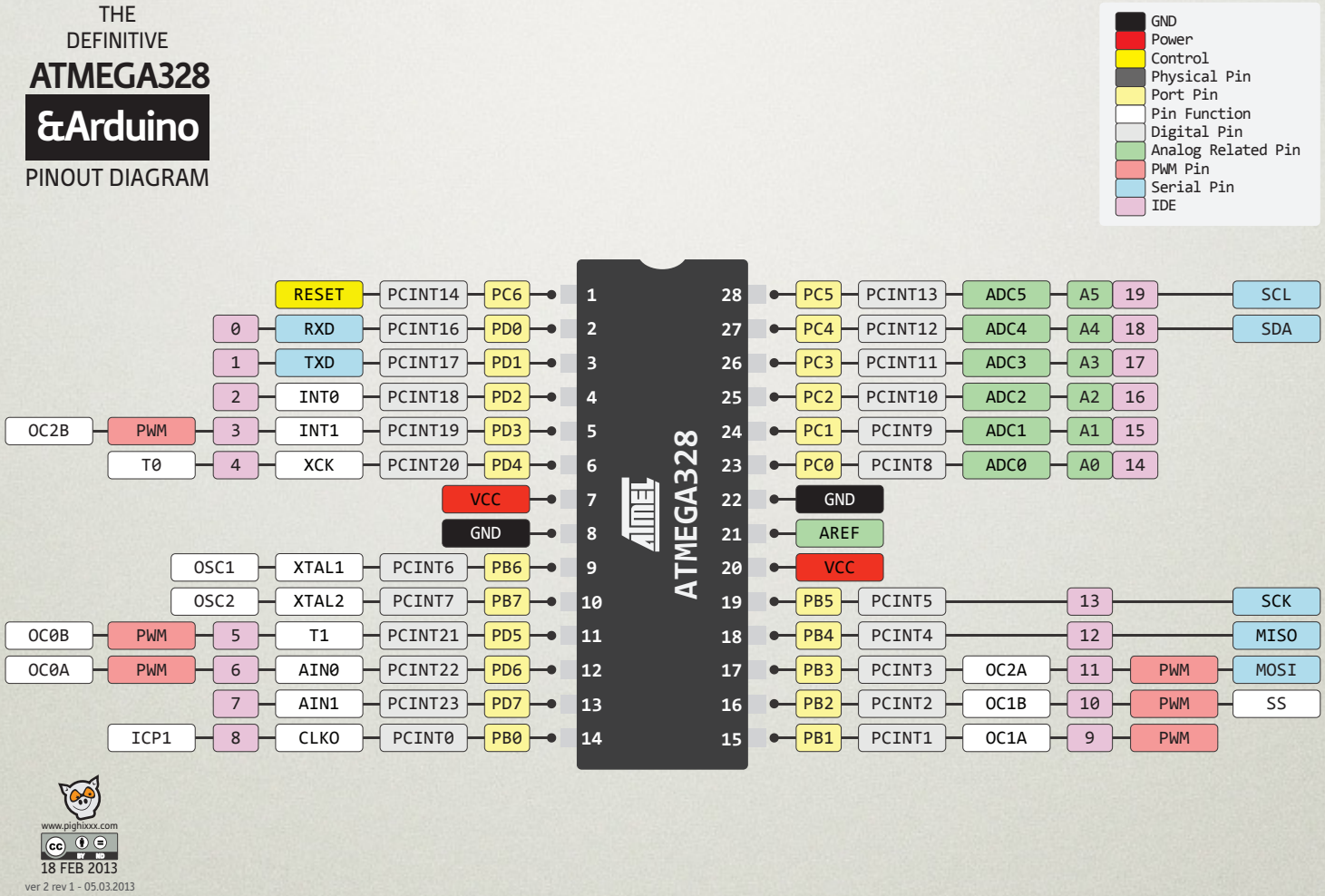
ATMEGA328 Internals



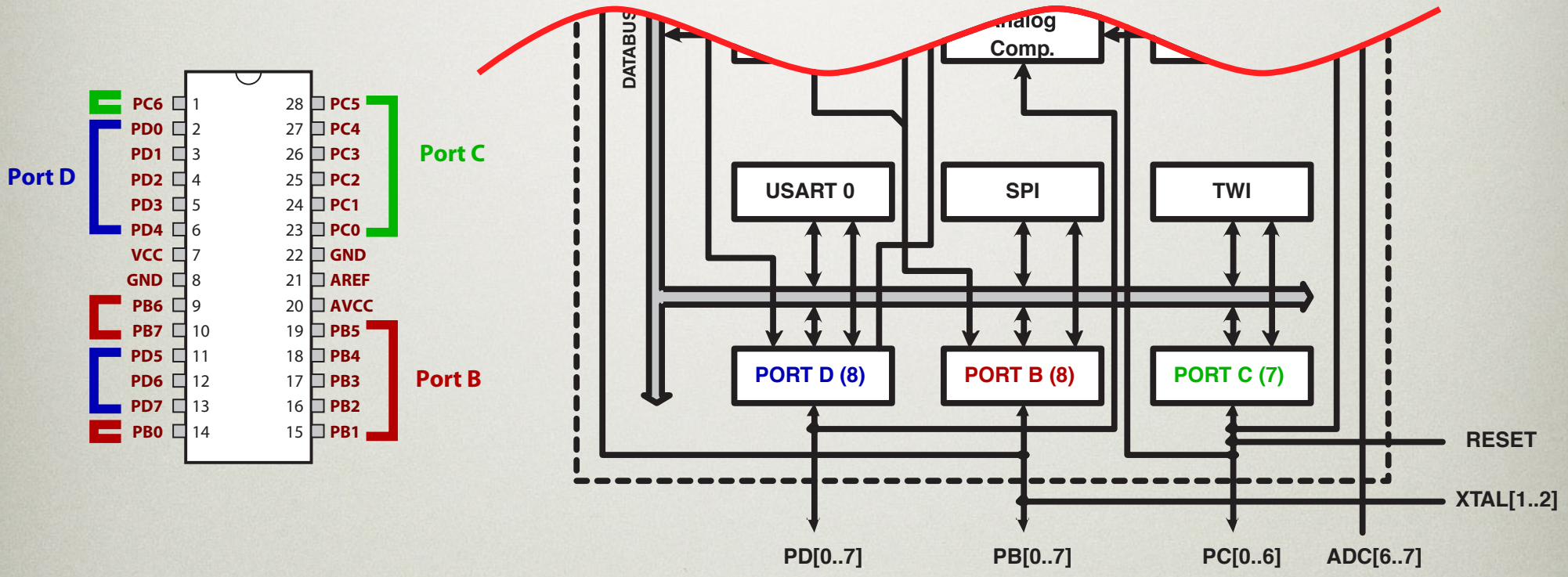
ATMega328 Features

- High Performance, Low Power AVR 8bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful instructions (many single clock cycle)
  - 32x8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20MIPS Throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 32Kb of In-System, Self-Programmable Flash program memory
  - 1Kb EEPROM
  - 2Kb Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data Retention: 20 years at 85C/100 years at 25C
  - Optional Boot Code Section with independent lock bits
  - Programming lock for Software Security
- Special Microcontroller features
  - Power-on Reset and programmable brown-out detection
  - Internal Calibrated oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with separate prescaler, compare mode, and capture mode.
  - Real Time counter with separate oscillator
  - Six PWM Channels
  - Six-channel 10-bit ADC, temperature measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (I^2C compatible)
  - Programmable Watchdog Timer with separate on-chip oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- I/O Lines: 23 Programmable I/O Lines
- Operating Voltage: 1.8-5.5v
- Temperature Range: -40C to 85C
- Power Consumption
  - Active Mode: 0.2mA
  - Power-down Mode: 0.1μA
  - Power-Save Mode: 0.75μA (including 32kHz RTC)

ATMega328 Pinout



ATMega328 Ports

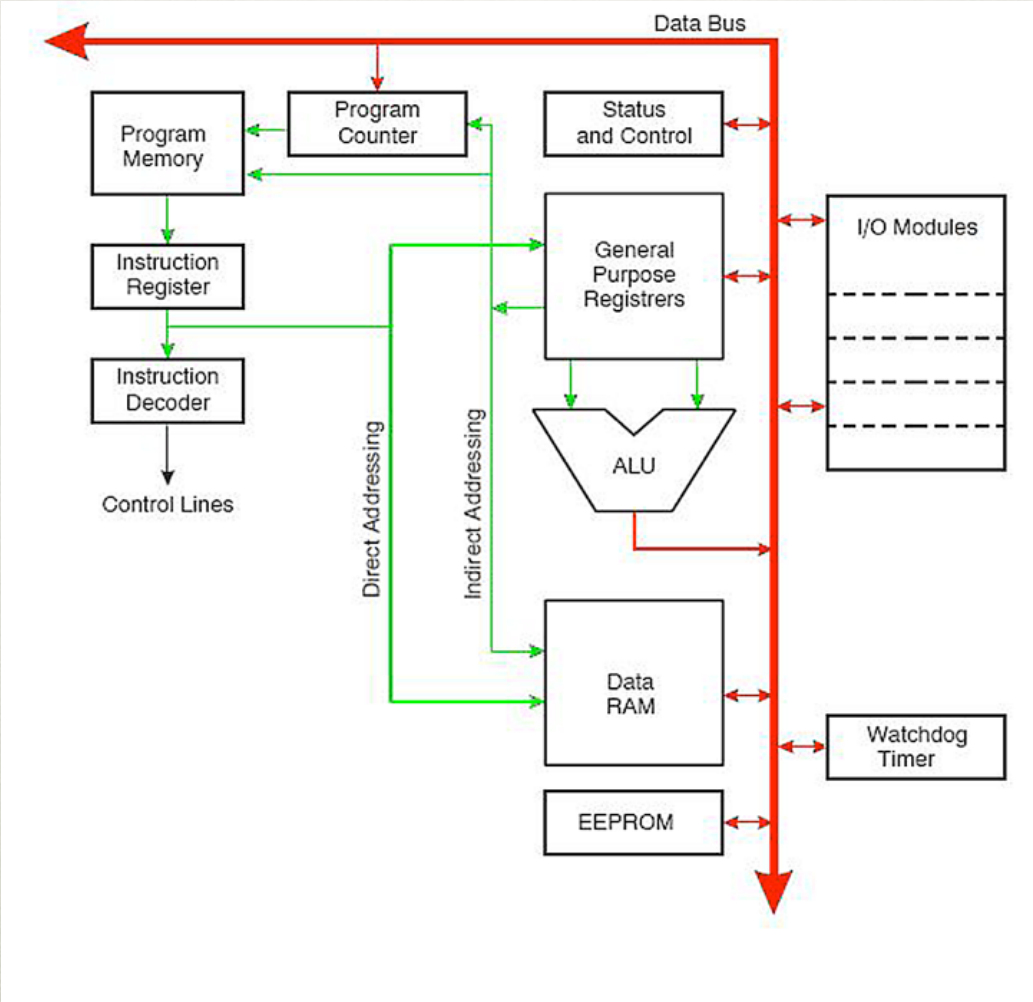


bidirectional ports

RISC Processor

- Reduced Instruction Set Computer
- As compared to Complex Instruction Set Computers, i.e. x86
- Assumption: Simpler instructions execute faster
- Optimized most used instructions
- Other RISC machines: ARM, PowerPC, SPARC
- Became popular in mid 1990s

Processor Layout



AVR Registers

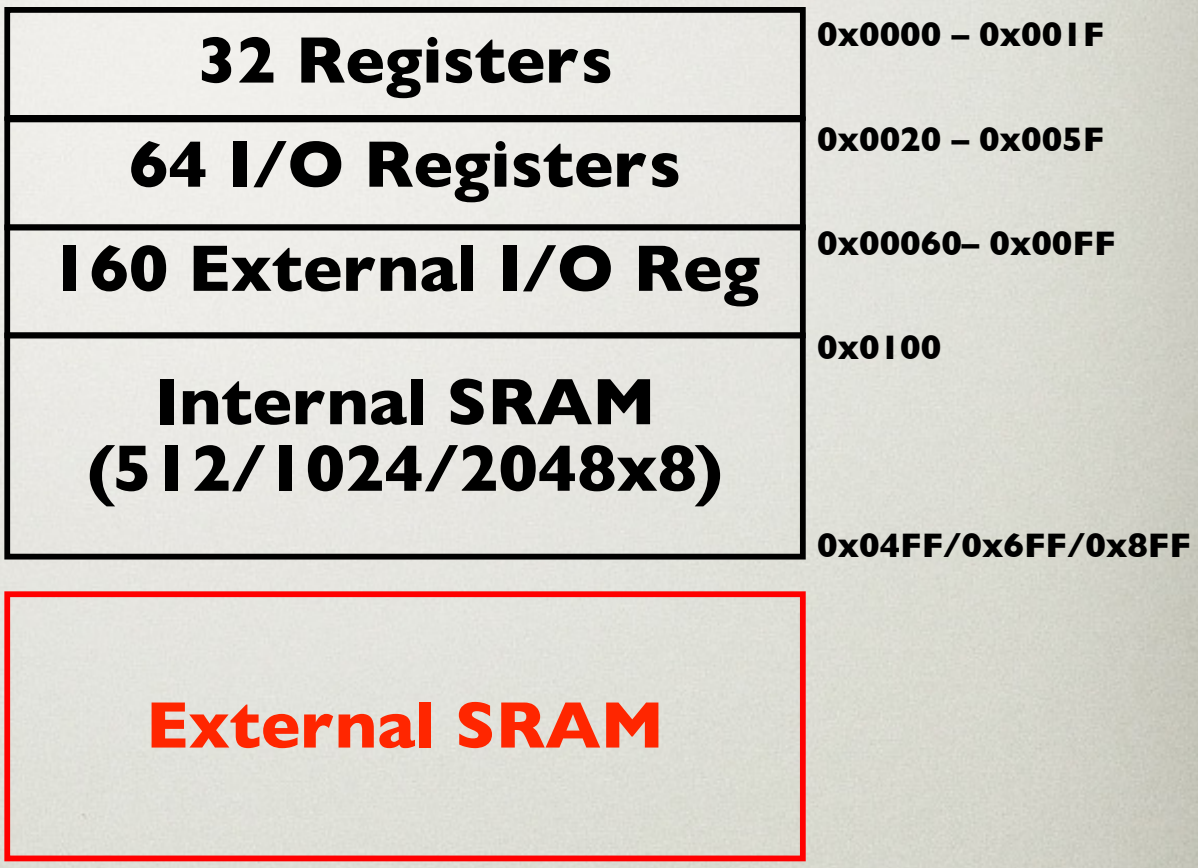
- 32 8 Bit registers
- Mapped to address 0-31 in data space
- Most instructions can access any register and complete in one cycle
- Last 3 register pairs can be used as 3 16 bit index registers
- 32 bit stack pointer

Flash Memory

- Non-volatile program space storage
- 16 Bit width
- Some devices have separate lockable boot section
- At least 10,000 write/erase cycles

AVR SRAM

- Data space storage
- 8 Bit width



AVR EEPROM

- Electrically Erasable Programmable Read Only Memory
- 8 bit width
- Requires special write sequence
- Non-volatile storage for program specific data, constants, etc.
- At least 100,000 write/erase cycles

Memory Mapped I/O Space

- I/O registers visible in data space
  - I/O can be accessed using same instructions as data
  - Compilers can treat I/O space as data access
- Bit manipulation instructions
  - Set/Clear single I/O bits
  - Only work on lower memory addresses

Arithmetic Logic Unit (ALU)

- Directly connected to all 32 general purpose registers
- Operations between registers executed within a single clock cycle
- Supports arithmetic, logic and bit functions
- On-chip 2-cycle Multiplier

131 Instructions

- Arithmetic & Logic
- Branch
- Bit set/clear/test
- Data transfer
- MCU control

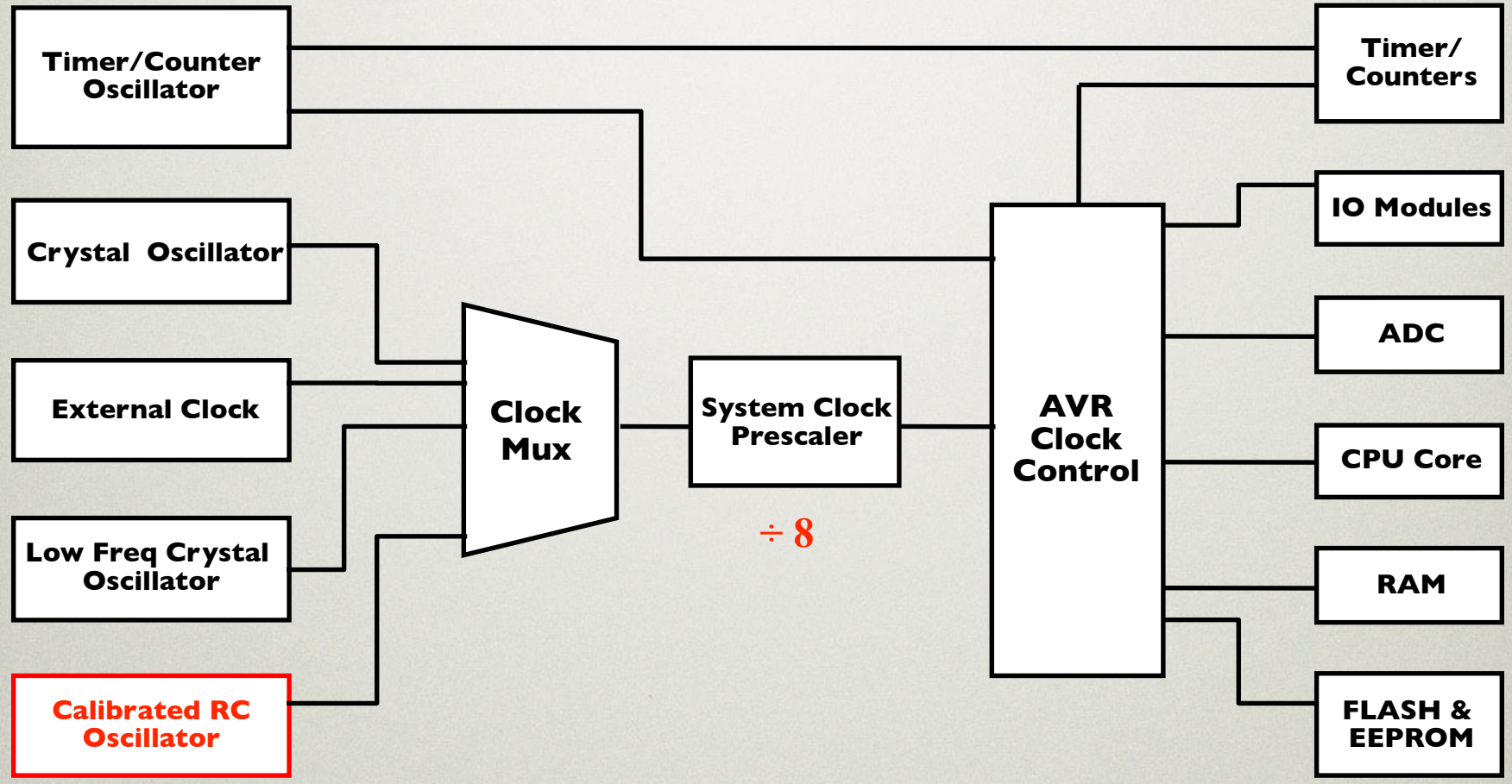
Instruction Timing

- Register ↔ register (1 cycle)
- Register ↔ memory (2 cycles)
- Branch instruction (1-2 cycles)
- Subroutine call & return (3-5 cycles)
- Some operations may take longer for external memory

AVR Clock System

- Clock control module generates clocks for memory and IO devices
- Multiple internal clock sources
- Provisions for external crystal clock source (max 20 MHz)
- Default is internal RC 8 MHz oscillator with ÷ 8 prescale yielding 1 MHz CPU clock
- Default is only 5-10% accurate

Clock Sources



Power Management

- Multiple power down modes
  - Power down mode
    - Wake on external reset or watchdog reset
  - Power save mode
    - Wake on timer events
  - Several standby modes
- Unused modules can be shut down

Reset Sources

- Power on reset
- External reset
- Watchdog system reset
- Brown out detect (BOD) reset

Interrupts

- ATmega328 has 26 reset/interrupt sources
- 1 Reset source
- 2 External interrupt sources
- I/O Pin state change on all 24 GPIO pins
- Peripheral device events

Interrupt Vectors

- Each vector is a 2 word jump instruction
- Vectors start at program memory address 0
- Reset vector is at address 0
- Sample vector table:

```
Address Labels        Code            Comments
0x0000                jmp RESET       ; Reset Handler
0x0002                jmp EXT_INT0    ; IRQ0 Handler
0x0004                jmp EXT_INT1    ; IRQ1 Handler
0x0006                jmp PCINT0      ; PCINT0 Handler
0x0008                jmp PCINT1      ; PCINT1 Handler
                      ...
```

Fuses

- Fuses configure system parameters
  - Clock selection and options
  - Boot options
  - Some IO pin configurations
  - Reset options
- Three 8 bit fuse registers
- Use caution! Some configurations can put the device in an unusable state!

ATMega Peripherals

- 23 General Purpose IO Bits
- Two 8 bit & one 16 bit timer/counters
- Real time counter with separate oscillator
- 6 PWM Channels
- 6 or 8 ADC channels (depends on package)
- Serial USART
- SPI & I2C (TWI) Serial Interfaces
- Analog comparator
- Programmable watchdog timer

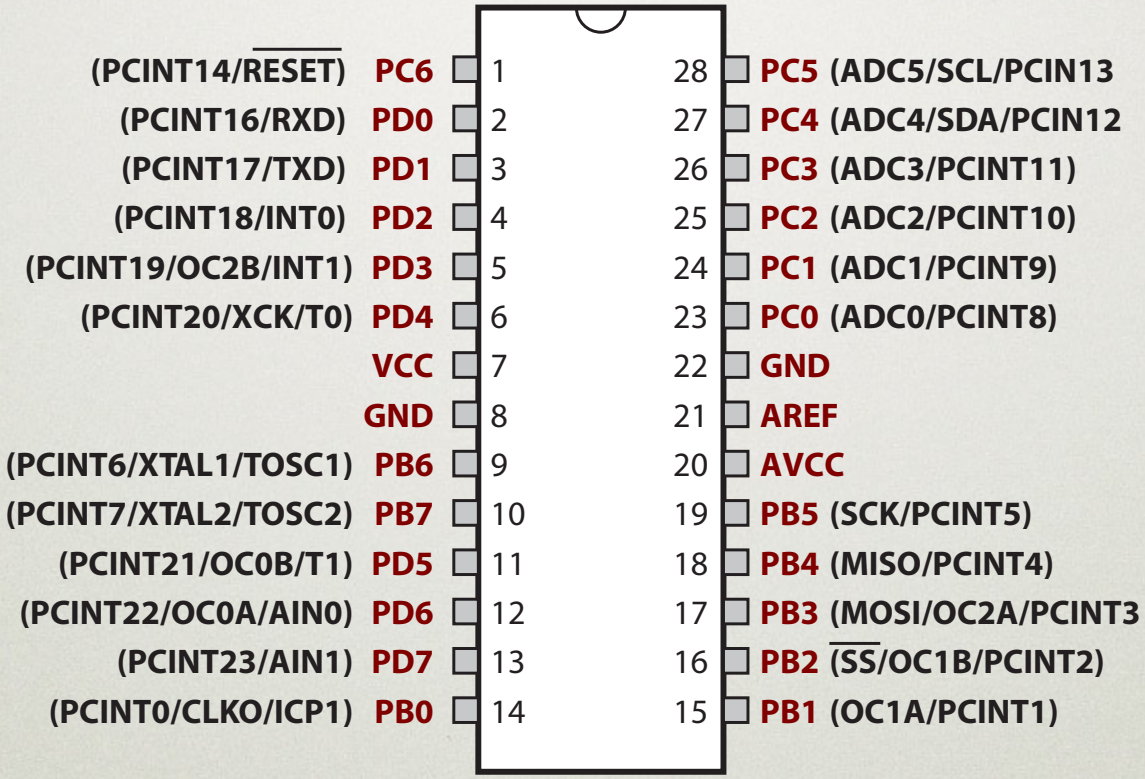
GPIO Ports

- Three 8 Bit IO Ports
  - Port B, Port C & Port D
  - Pins identified as PBx, PCx or PDx (x=0..7)
- Each pin can be configured as:
  - Input with internal pull-up
  - Input with no pull-up
  - Output low
  - Output high

Alternate Port Functions

- Most port pins have alternate functions
- Internal peripherals use the alternate functions
- Each port pin can be assigned only one function at a time

Alternate Pin Usage



(see Appendix A)

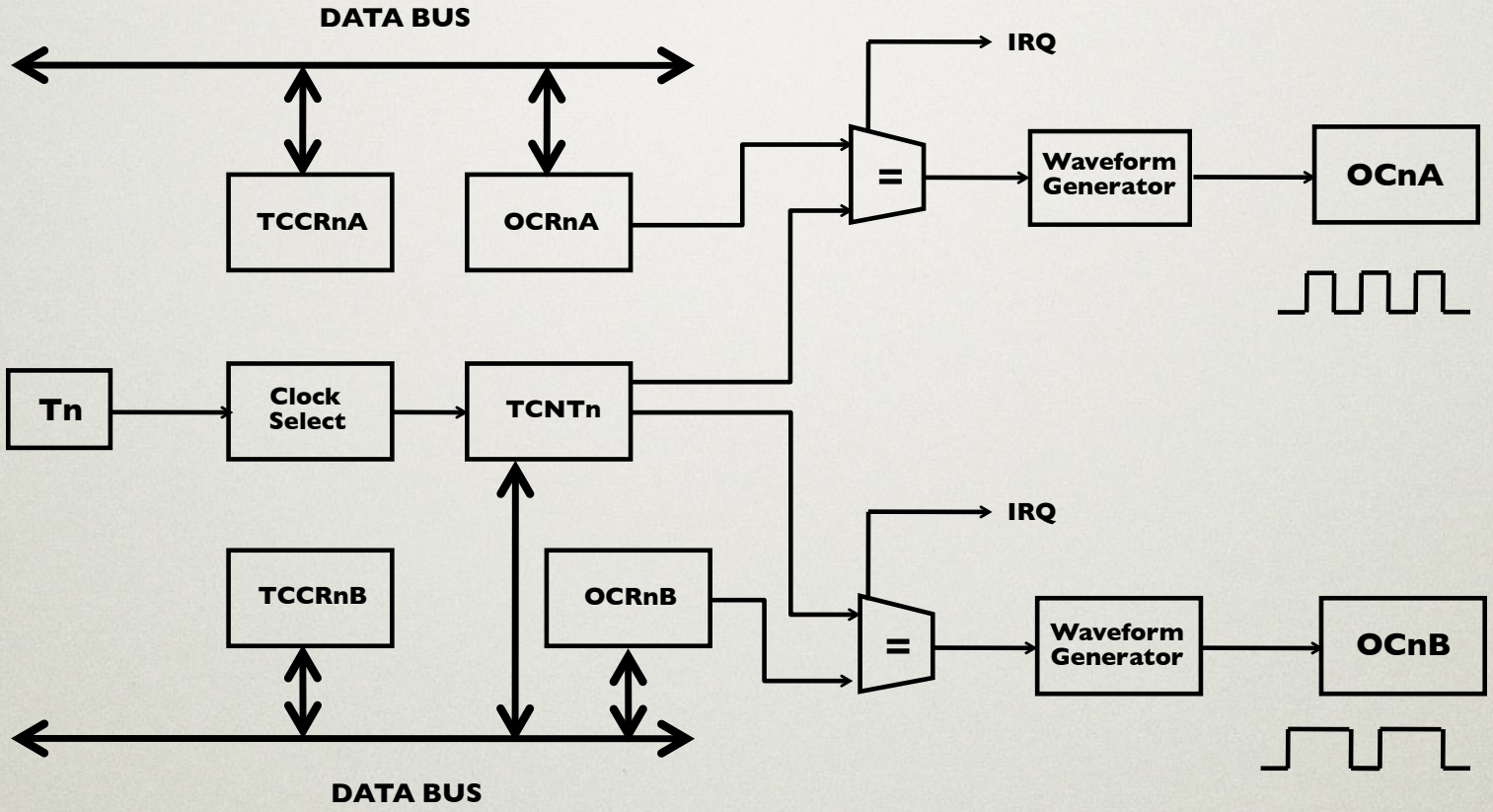
Timers/Counters

- 8/16 Bit register
  - Increments or decrements on every clock cycle
  - Can be read on data bus
  - Output feeds waveform generator
- Clock Sources
  - Internal from clock prescaler
  - External Tn Pin (Uses 1 port pin)

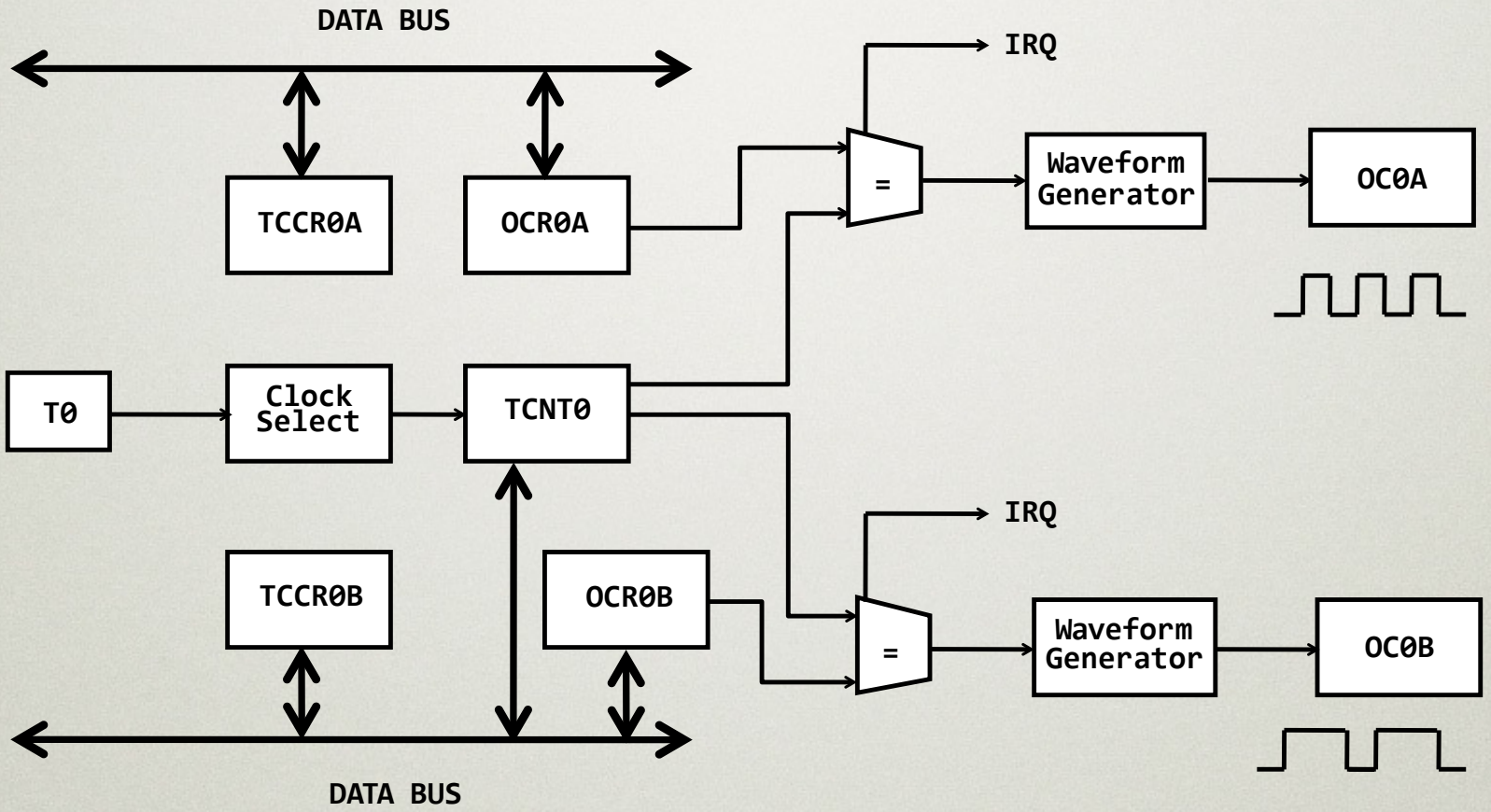
Timers/Counters

- Multiple Operating modes
  - Simple timer / counter
  - Output Compare Function
    - Waveform generator
      - Clear/set/toggle on match
    - Frequency control
    - Pulse Width Modulation (PWM)

Timer/Counter Block Diagram

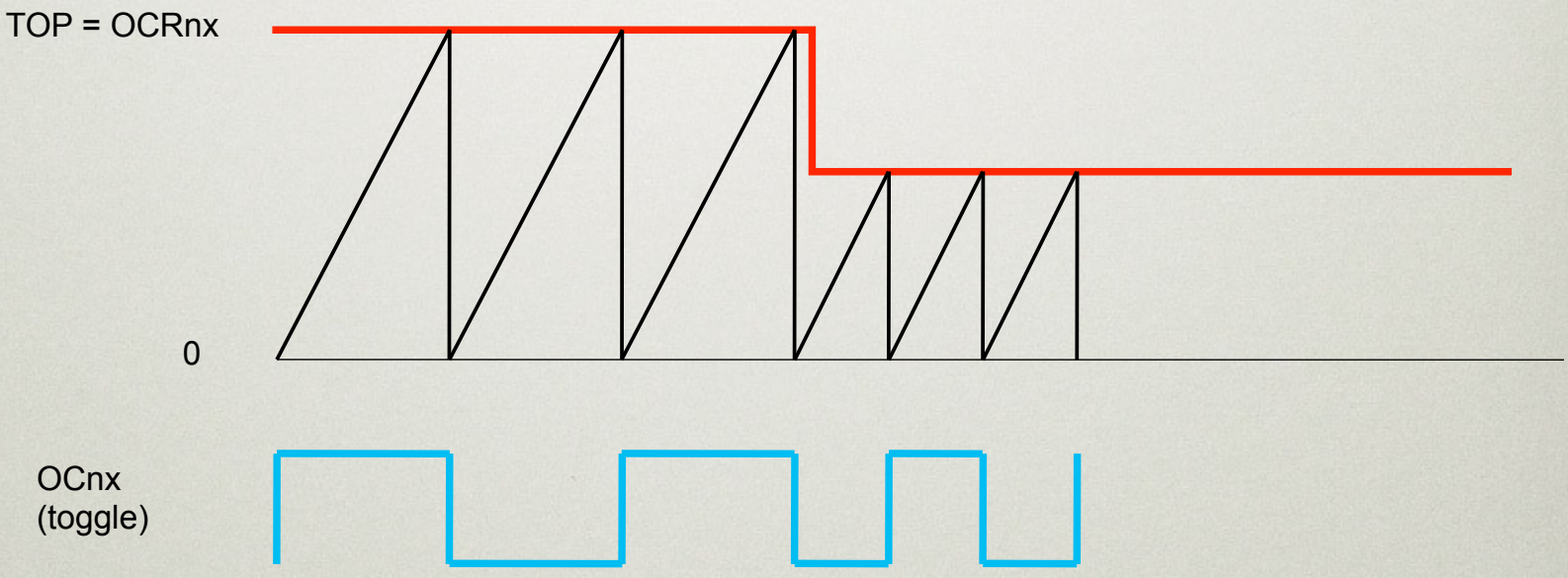


Timer/Counter 0 Block Diagram



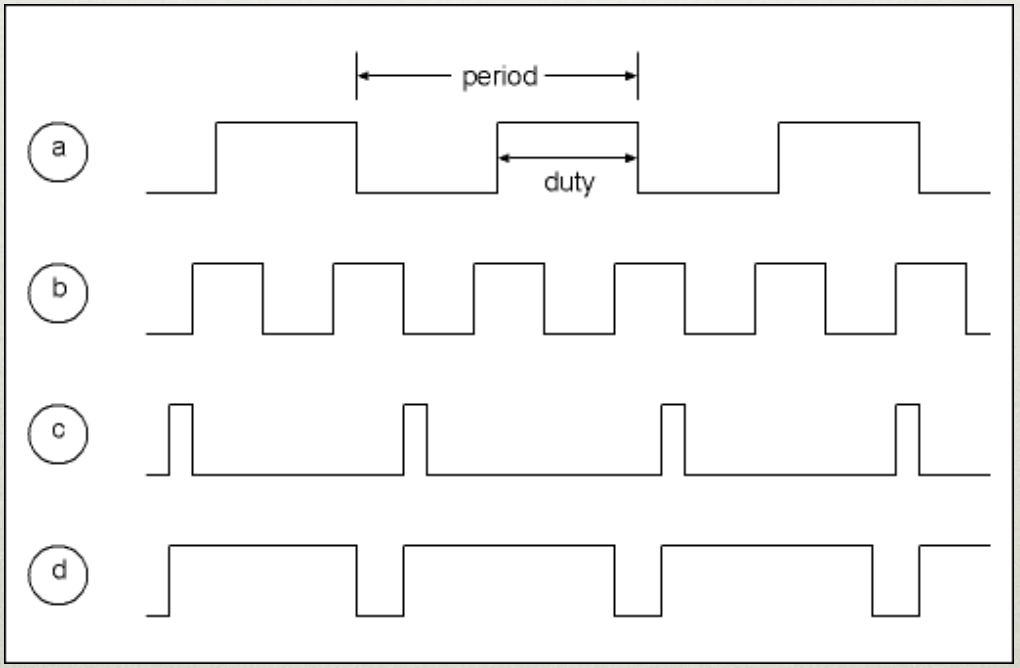
Controlling the Frequency

- Use Clear Timer on Compare Match (CTC) Mode
- OCnx Toggles on Compare Match



Pulse Width Modulation (PWM)

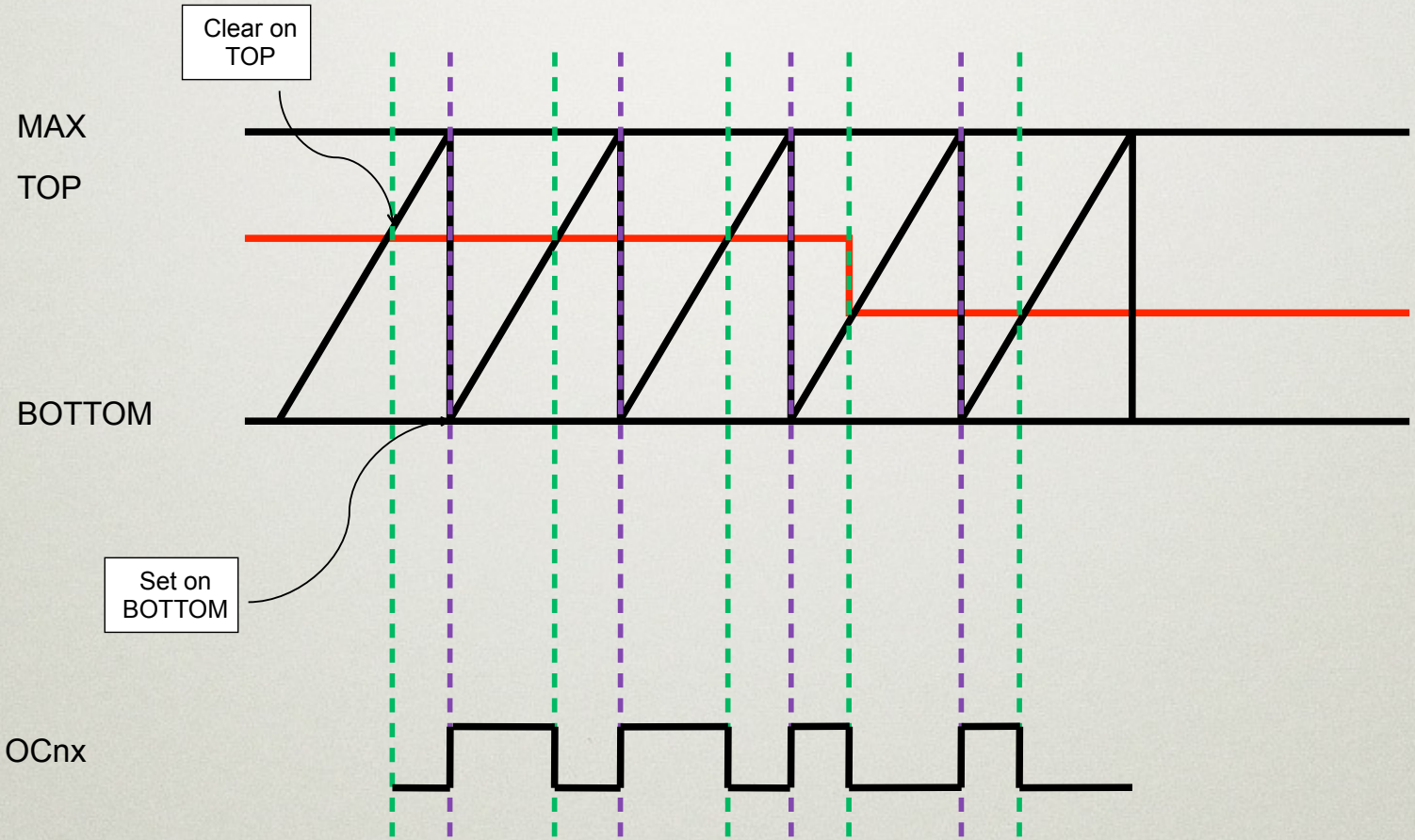
- **Dynamically change duty cycle of a waveform**
- **Used as a form of *analog out*.**



Fast PWM Mode

- Counter counts from BOTTOM (0) to MAX
- Counter reset to 0 at MAX
- OCnx cleared at TOP
- OCnx set at BOTTOM

PWM Waveform Generation



Timer 1 Capture Mode

- Capture can be triggered by ICP1 pin or ACO from analog comparator
- Capture event copies timer into input capture register ICR1
- Can be used to time external events or measure pulse widths (time-stamp)
- Range finders generate pulse width proportional to distance

Analog-To-Digital Convertor

- 10 Bit Successive Approximation ADC
- 8 Channel multiplexer using port pins ADC0-7
- Max conversion time 260 μsec.

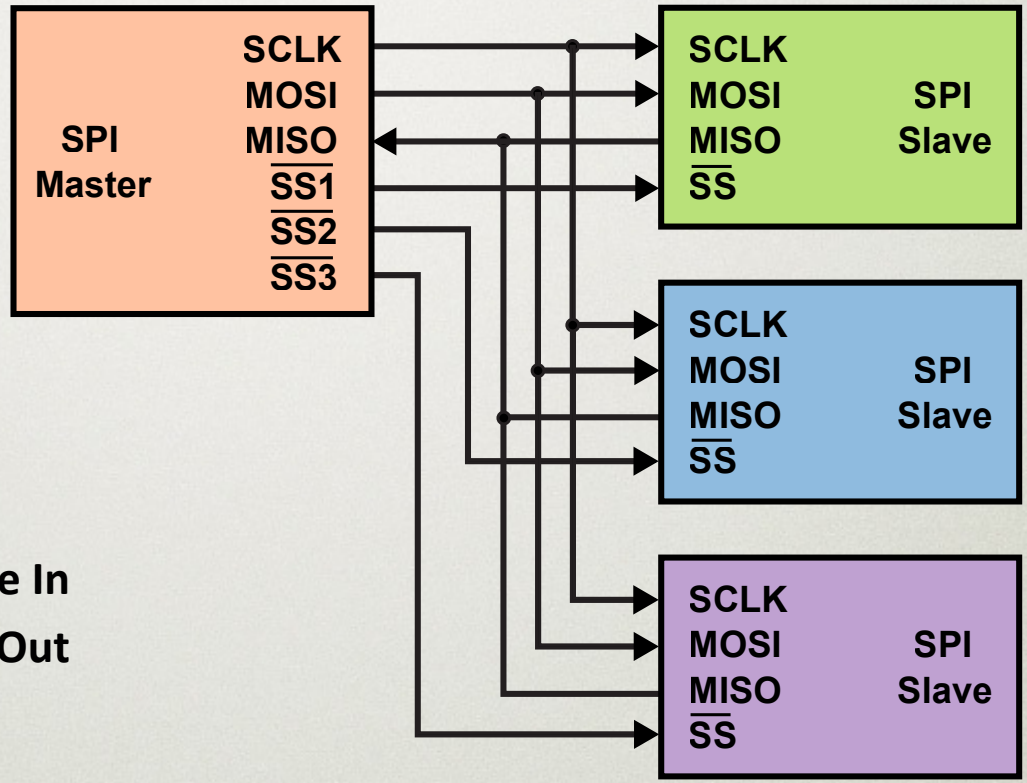
Analog Comparator

- Compares voltage between pins AIN0 and AIN1
- Asserts AC0 when AIN0 > AIN1
- AC0 can trigger timer capture function
  - Range finders indicate distance with pulse width
  - Timer capture mode can compute pulse width

Serial Peripheral Interface (SPI)

- **Industry standard serial protocol for communication between local devices**
- **Master/Slave protocol**
- **3 Wire interface**
- **Slaves addressed via Slave Select (SS) inputs**

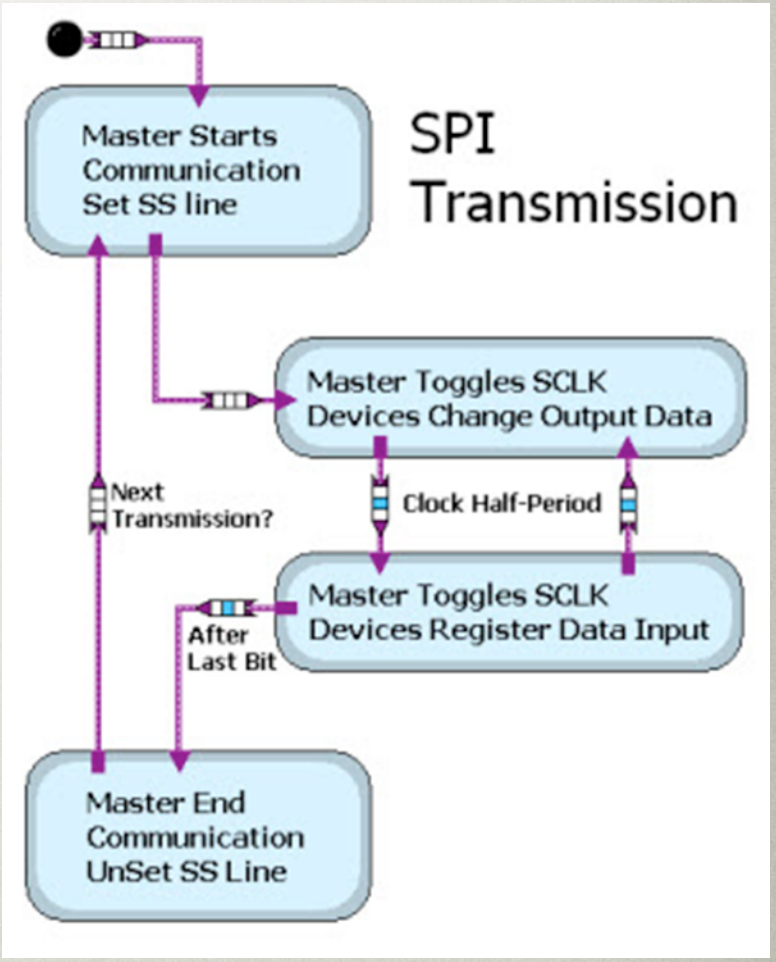
SPI Bus Signals



SCLK	Serial Clock
MOSI	Master Out Slave In
MISO	Master In Slave Out
SS	Slave Select

SPI Bus Operation

- The Master drives a particular SS line
- The SCLK signals the device to set the MOSI and MISO
- Specified number of bits transmitted
- the Master pulls the SS line for the slave back high

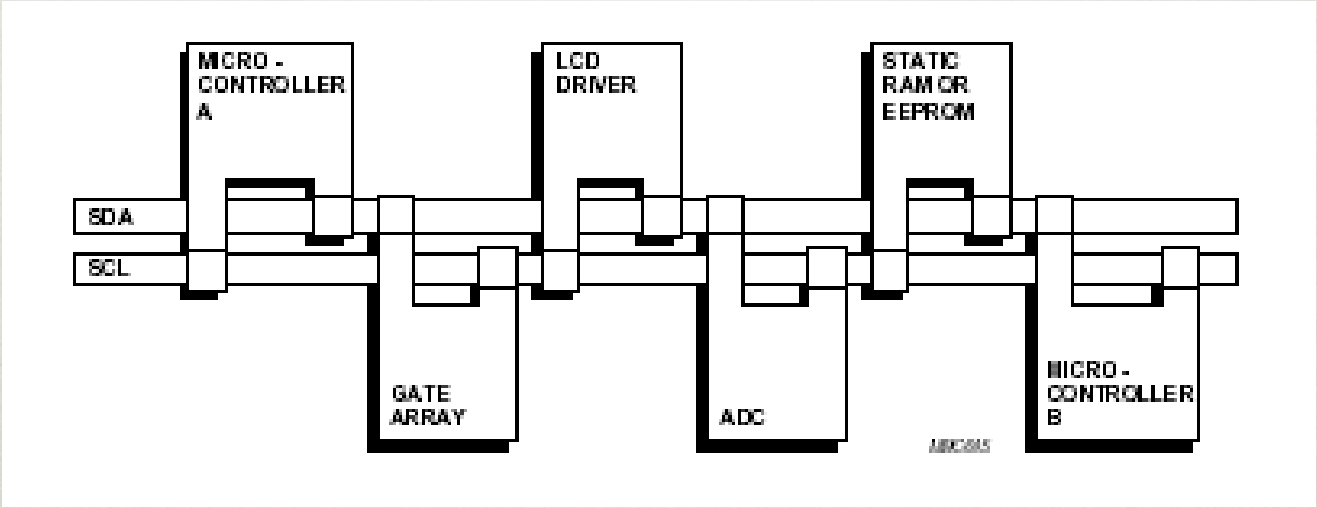


I²C Bus Interface

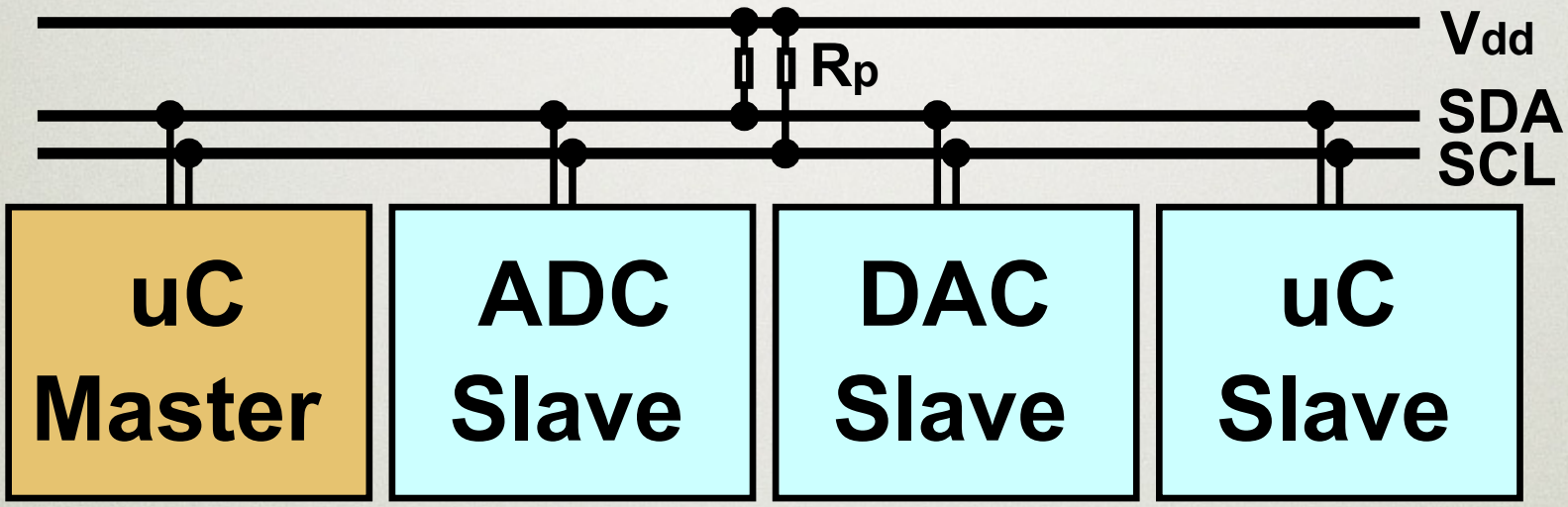
- Industry standard serial protocol for communication between local devices
- Master/Slave protocol
- 2 Wire interface (TWI)
- Byte oriented messages
- Slave address embedded in command

I²C Bus Signals

SDA	Serial Data
SCL	Serial Clock



I²C Bus Connections



SPI and I²C Bus Applications

- EEPROM
- IO Expanders
- Real Time Clocks
- ADC & DAC
- Temperature sensors
- Ultrasonic range finders
- Compass
- Servo / Motor Controller
- LED Display

USART

- Universal Synchronous and Asynchronous (serial) Receiver and Transmitter
- Full Duplex Operation
- High Resolution Baud Rate Generator
- Can provide serial terminal interface